Last DSM Algorithm
2006 Version

8th March 2005

Input Bits

Input Channel	Bit Description
0	Unused
1	VTX Information Bit 0 – BBC TAC difference in window Bit 1 – Unused Bit 2 – BBC East small-tile ADC sum over threshold 0 Bit 3 – BBC West small-tile ADC sum over threshold 0 Bits 4:9 – Unused Bit 10 – MTD trigger Bits 11:15 - Unused
2	Unused
3	EMC Information Bits 0:1 – BEMC Jet Patch threshold bits Bits 2:3 – BEMC high-tower threshold bits Bit 4 – BEMC energy sum threshold bit Bit 5 – J/Ψ-bit from BEMC-high towers Bit 6 – BEMC HT.TP combined threshold bit Bits 7:8 – EEMC Jet Patch threshold bits Bits 9:10 – EEMC high-tower threshold bits Bit 11 – EEMC energy sum threshold bit Bit 12 – EEMC HT.TP combined threshold bit Bits 13:14 – Unused Bit 15 – BEMC+EEMC total energy sum threshold bit
4	Miscellaneous Information Bit 0 – Blue bunch filled Bit 1 – Yellow bunch filled Bits 2:15 - Unused
5	FPD Information Bit 0:7 – to be updated Bits 8:15 - Unused
6	Special Trigger Requests Bits 0:13 - Unused Bit 14 – Zero-bias bit Bit 15 - Unused
7	Unused

Registers

Register	Register Description
0	2-bit integer for selecting one of the three energy sum bits
1	8-bit minimum bias prescale counter
2	8-bit mask for FPD1
3	8-bit mask for FPD2

Output Bits

Bit	Description
Bits 0:15	
0	MTD trigger
1	FPD1
2	FPD2
3	EMC ETOT
4	J/Ψ trigger
5	BEMC HT.TP combined threshold bit
6	BEMC HT>threshold 2
7/8	BEMC jet-patch bits (coding three thresholds)
9	EEMC HT.TP combined threshold bit
10	EEMC HT>threshold 2
11/12	EEMC jet-patch bits (coding three thresholds)
13	Prescaled minimum bias trigger
14	Minimum bias trigger
15	Zero bias trigger
Bits 16:31	Same definitions as bits 0:15

Internal Logic

- The two FPD-related bits are created in parallel using independent masks:
  The 8-bit FPD input is fanned out to 2 separate copies: set-1 and set-2
  Each set is then masked with its own mask: set-1 is masked with register 2 and set-2 is masked with register 3
  The bits in each masked set are then OR'ed together to create FPD1 and FPD2
  i.e. FPD1 = (masked set-1 bit 0) OR (masked set-1 bit 1) OR (masked set-1 bit 2) OR etc…
  FPD2 = (masked set-2 bit 0) OR (masked set-2 bit 1) OR (masked set-2 bit 2) OR etc…

- One of the three input energy sums is selected, using Register 0, for output bit 3:
  Register 0 = 0: output bit 3 = 0
  Register 0 = 1: output bit 3 = BEMC energy sum threshold bit
  Register 0 = 2: output bit 3 = EEMC energy sum threshold bit
  Register 0 = 3: output bit 3 = BEMC+EEMC energy sum threshold bit

- The minimum bias trigger bit is set when the following condition is met:
  BBC East small-tile ADC sum over threshold 0 AND
  BBC West small-tile ADC sum over threshold 0 AND
  BBC TAC difference in window AND
  Blue bunch filled AND
  Yellow bunch filled
  NOTE: The BBC components of the minimum bias definition are based on thresholds applied earlier in the DSM tree. If the user wants to remove one of these components then this can be achieved by setting those thresholds to their lowest and/or highest values (whichever is appropriate). However, there is no way in software to remove the blue and yellow component.

- Whenever the minimum bias condition is met the minimum bias prescale logic is also activated. The prescale counter starts from the value set in register 1 and decrements that value by 1 every time the minimum bias condition is met. If the value has already reached 1 then it is reset to the starting value. In parallel, when the counter value is 1 the prescaled minimum bias trigger bit is set. Presacle values between 1 and 255 can be specified in register 1.